Future Proofing your MicroTCA design for Serial RapidIO 2.0

George Song
Sr. Application Engineer
IDT
(george.song@idt.com)

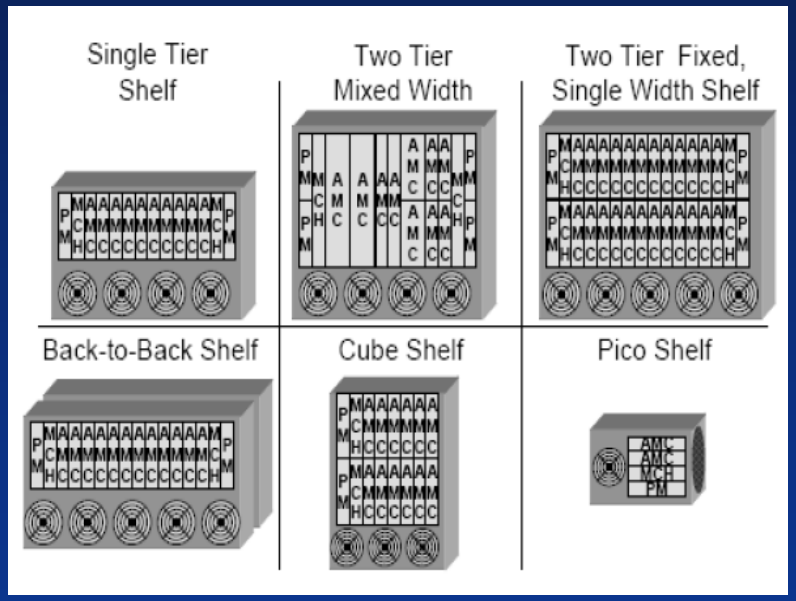
Agenda

- MicroTCA Introduction
- sRIO 2.0 vs sRIO 1.3
- Valuable sRIO 2.0 features for a sRIO 1.3/2.0 mixed system
- Future Proofing your modular MicroTCA design for sRIO 2.0 tomorrow
- IDT- Leading the transition to sRIO 2.0

MicroTCA Introduction

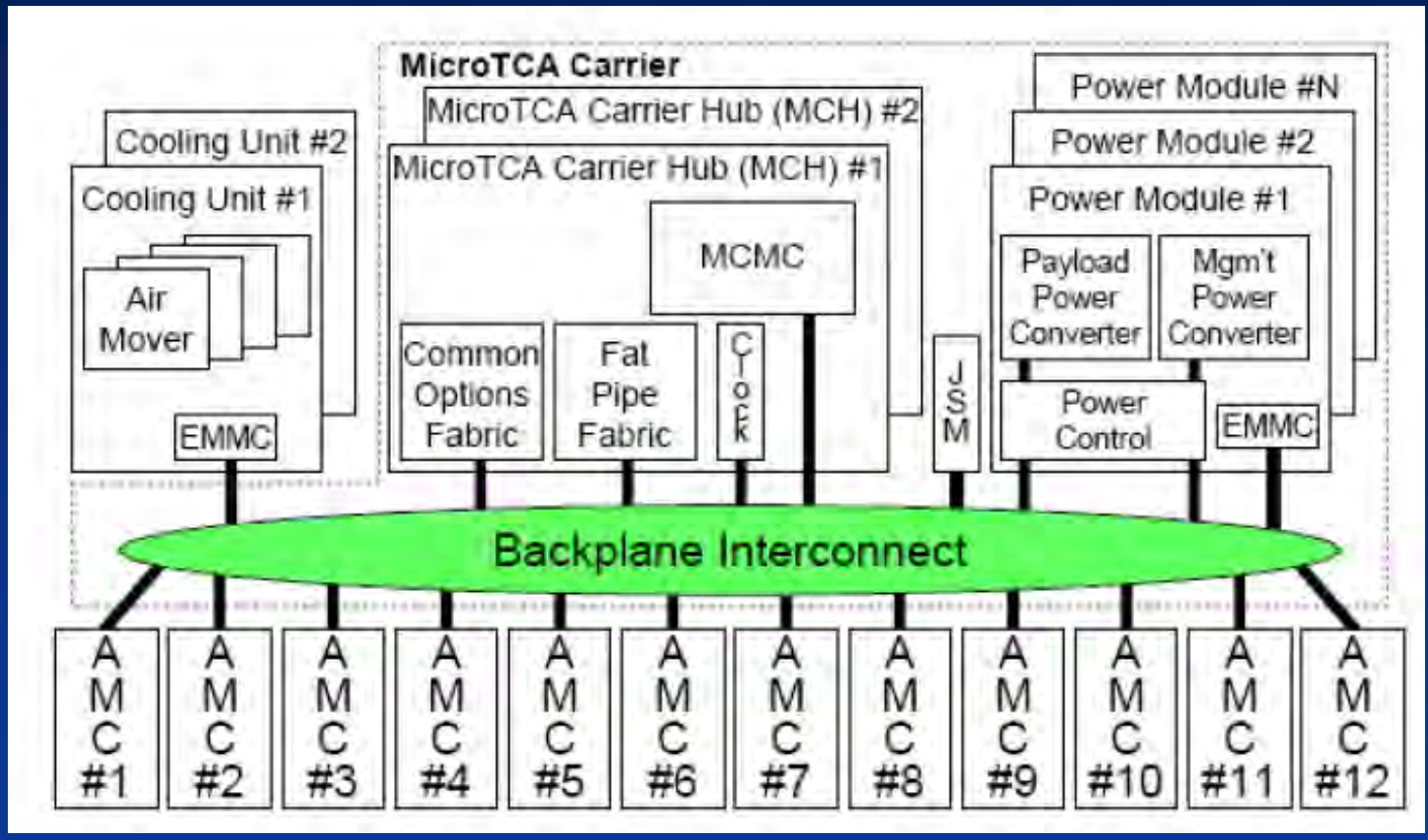
MicroTCA Typical Applications

- **Base stations**
- **VoIP gateways**
- **WiMAX solutions**
- **IP telephony**
- **IP TV**
- **Media servers**

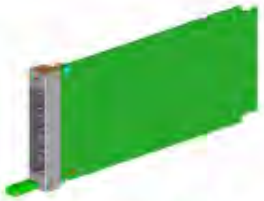
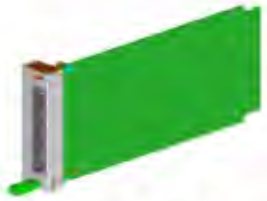


Six MicroTCA packaging illustrations

MicroTCA System Block Diagram

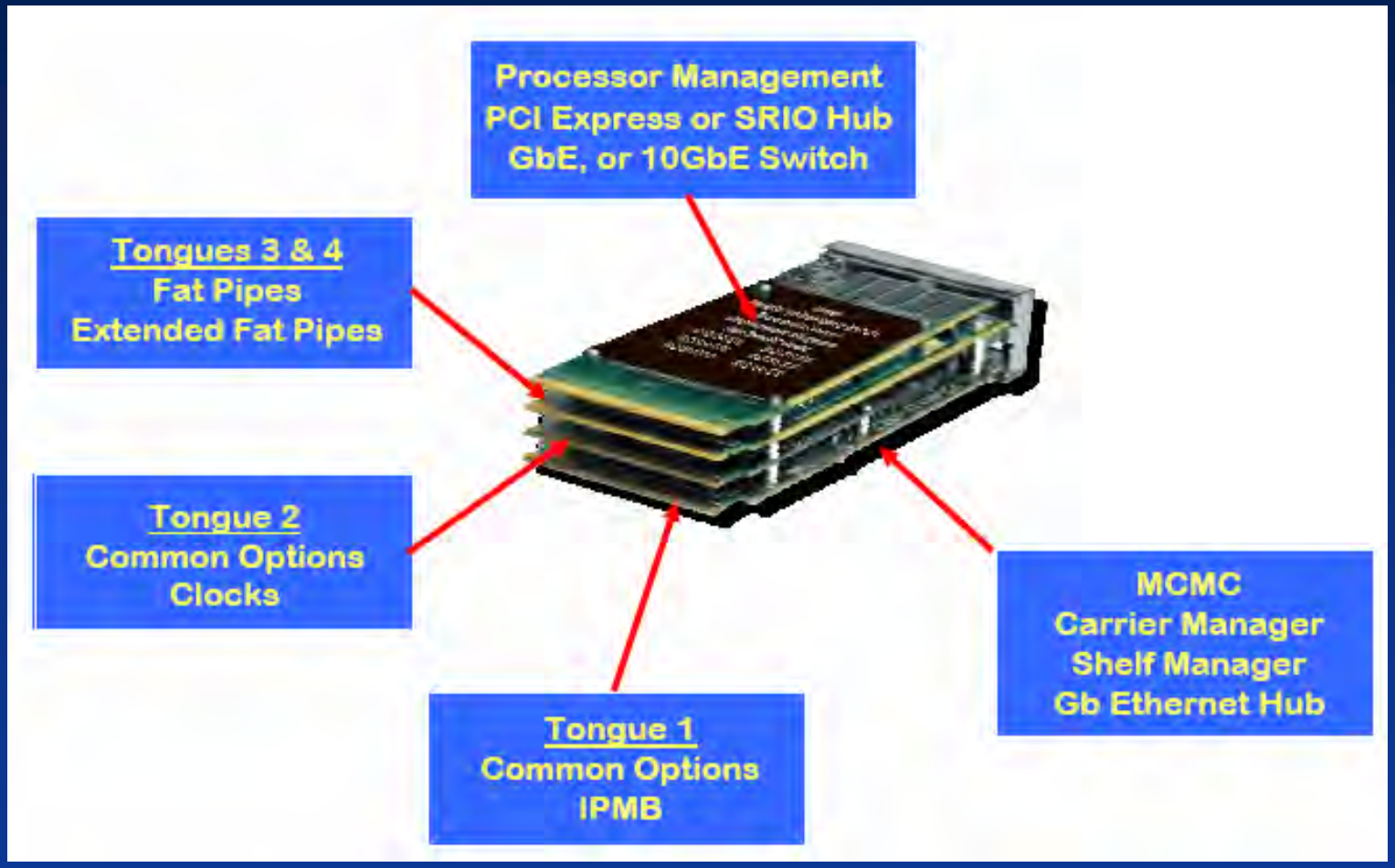


AdvancedMCs --- the primary component

	Compact-Size (3HP)	Mid-Size (4HP)	Full-Size (6HP)
Single modules	 73.8x13.88x181.5mm	 73.8x18.96x181.5mm	 73.8x28.95x181.5mm
Double modules	 148.8x13.88x181.5mm	 148. 8x18.96x181.5mm	 148. 8x28.95x181.5mm

AdvancedMC Module configuration examples

MicroTCA Carrier Hub



MicroTCA Interconnect Protocols

- PCI Express (AMC.1)
- Ethernet (AMC.2)
- Storage Interfaces (AMC.3)
- RapidIO (AMC.4)
- Future subsidiary specifications of AdvancedMCs

sRIO 2.0 vs sRIO 1.3

New Serial Physical Layer Feature Overview

sRIO v1.3

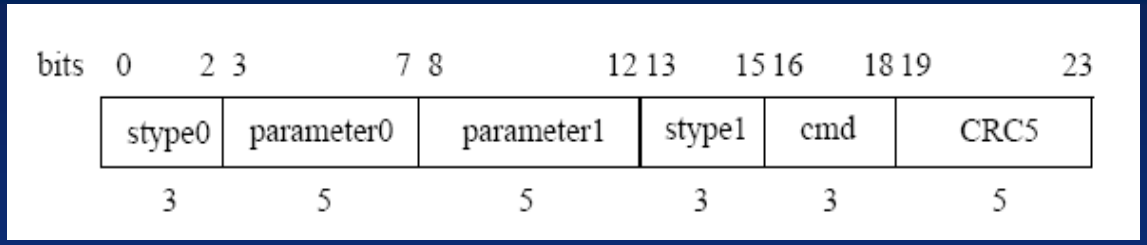
- Link width --- 1x, 4x
- Link rates --- 1.25, 2.5, 3.125 Gbaud XAUI
  - Long reach --- 50cm + 2 connectors
  - Short reach --- 20cm + 1 connectors

sRIO v2.0

- Link width --- 1x, 2x, 4x, 8x, 16x
- Link rates ---
  - 1.25, 2.5, 3.125 Gbaud XAUI
  - 5.0, 6.25 Gbaud OIF
    - Long reach --- 100cm + 2 connectors
    - Medium reach --- 60cm + 2 connectors
    - Short reach --- 20cm + 1 connector
    - Decision Feedback Equalization (DFE)
    - Data scrambling capability

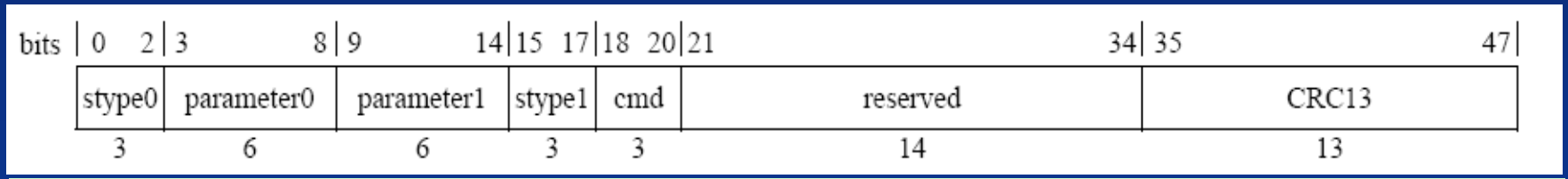
New Control Symbol and Idle Sequence

sRIO v1.3



- 24bits control symbol
- 5bits CRC

sRIO v2.0



- 48bits control symbol allows for Virtual Output Queue
- 13bits CRC for better DFE based receiver
- Idle provides auto detection of lane polarity, port width/lane number, data rate
- Idle provides auto-tuning of Transmitter emphasis setting

sRIO 2.0 Data Plane Enhancement Overview

Addition of Virtual Channels (VC) to Serial Physical Layers

- Continuous Traffic or reliable Traffic
- Allows reserving of bandwidth and Quality of Service (QoS) on subchannel granularity

New Data Streaming Packet Format (Type 9)

- Add support for end-to-end flow control
- Support On/Off, Rate based, and credit based schemes

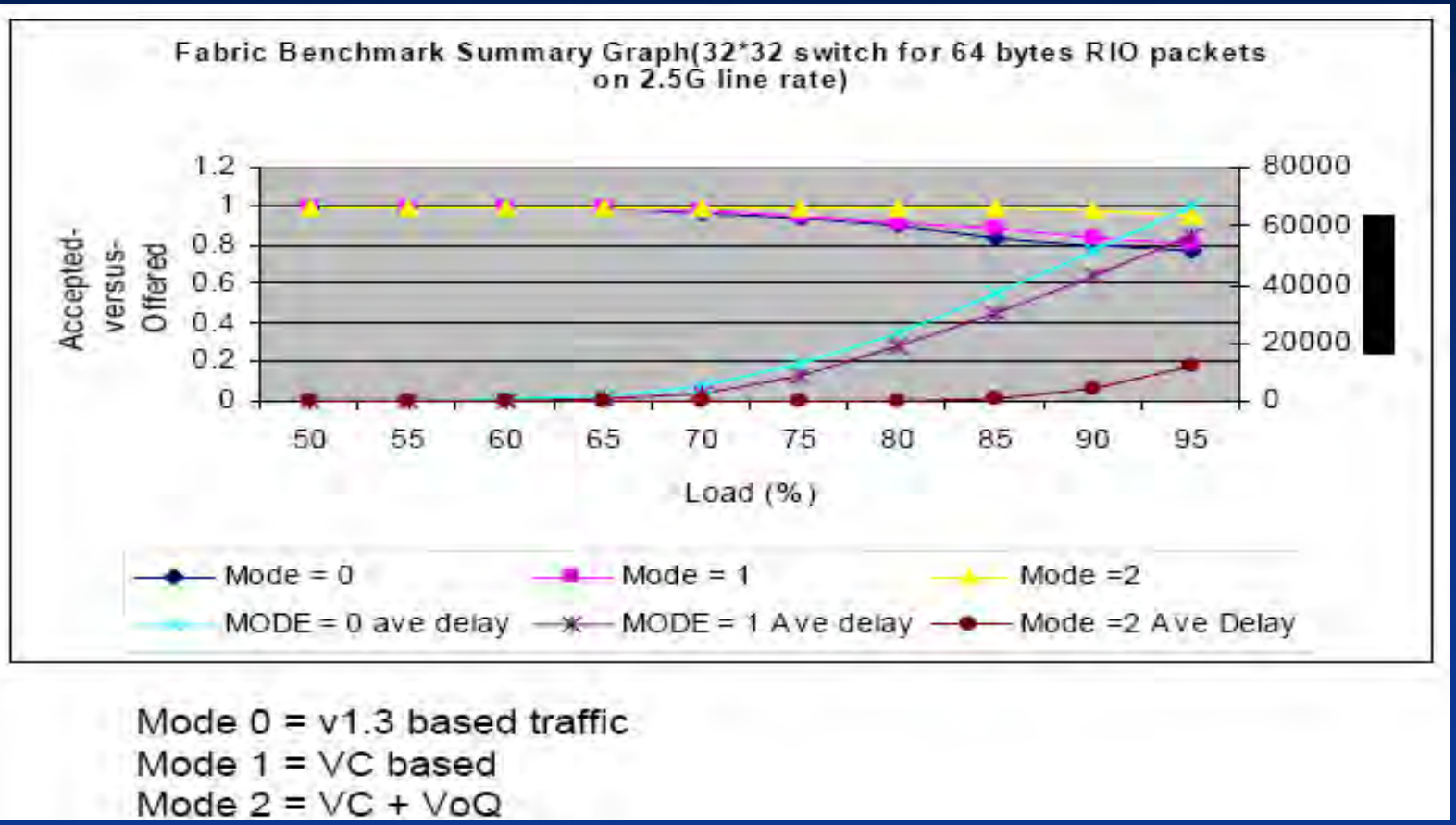
Virtual Output Queue (VoQ) Spec

-Two-stage virtual output table support to avoid Head-of-line (HOL) blocking
- Utilize new control symbol to communicate the congestion info about downstream ports

New Endpoint Flow Control Arbitration (Enhanced Type 7)

- Allows endpoints to manage and arbitrate for resource Segmentation and Reassembly (SAR) contents at a PDU level

Fabric Benchmark Improvement with VC and VoQ



Mode 0 = v1.3 based traffic
Mode 1 = VC based
Mode 2 = VC + VoQ

Courtesy of Chunhua Hu. Erlang Technologies

Summary of sRIO 2.0 Enhancements

- Higher Bandwidth, Maintaining Low Overhead
- Complete Set of Transactions
  - I/O
  - Messaging
  - Globally Shared Memory
  - Streaming Data
- Carrier Grade Data Fabric Performance
  - Deterministic Latency
  - Quality of Service
  - End to End Data Management
- Standardization of Encapsulation

Valuable sRIO 2.0 features for a sRIO 1.3/2.0 mixed system

Bandwidths Scheduling Rules of sRIO 2.0

Rules	Object
Bandwidth Reservation	VC0, VC1~VC8
Strict Priority	VC0

VC0 = bandwidth reservation →
- all VCs will receive their expected minimum bandwidth

VC0 = strict priority →
- VC0 will get whatever bandwidth it needs
- Remaining VCs will divide up whatever portion of bandwidth remains

When a VC demands less than its guaranteed bandwidth →
- Other VCs can use the available bandwidth

Packet Transmission Modes of sRIO 2.0

Reliable Transmission (RT)

- RT operations are like earlier versions of sRIO in that retransmitting a packet when it cannot be received makes packet transmission lossless.
- VC0 supports all defined priorities and operates exclusively in RT mode

Continuous Transmission (CT)

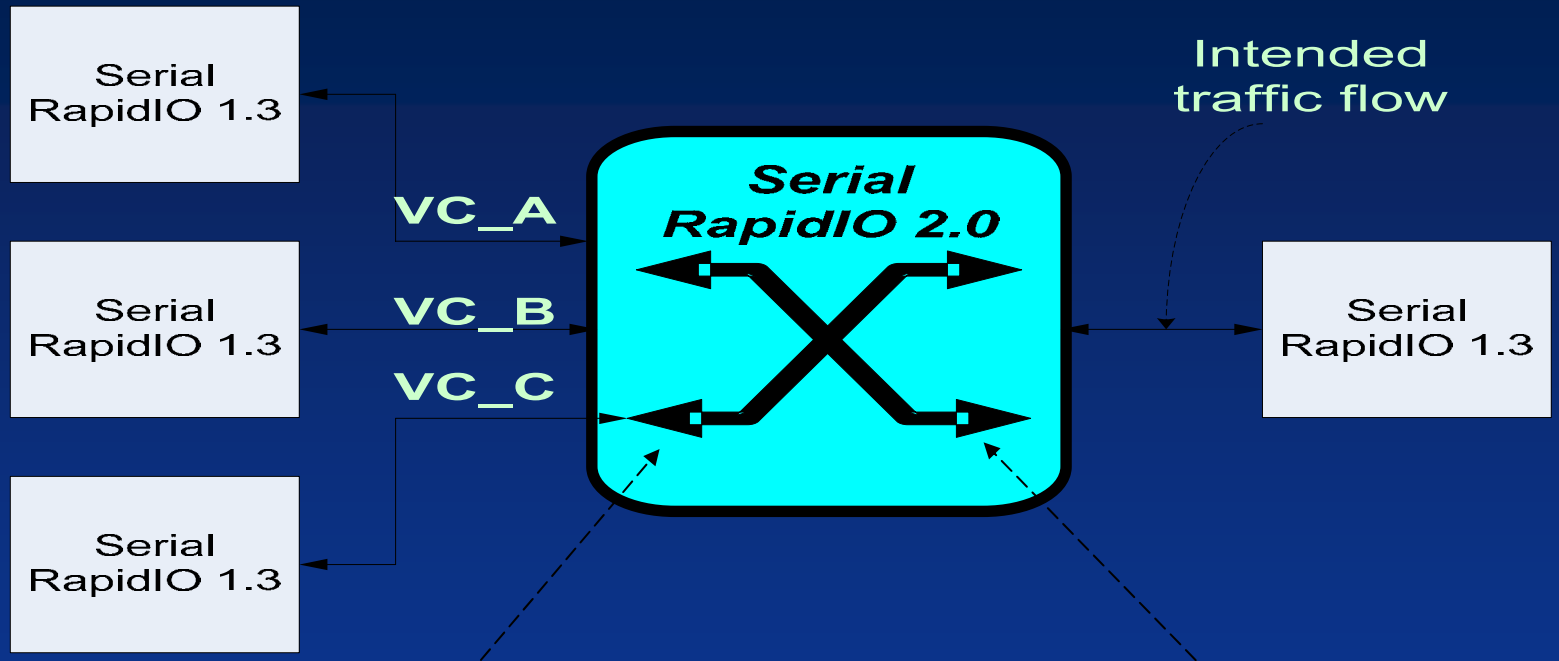
- CT is optimized to achieve low latency for traffic flows that can accommodate packet loss by not performing retransmissions.
- Higher VCs (1~8) can operate in CT or RT mode.

sRIO 1.x/2.0 Mixed System

- sRIO 1.x and sRIO 2.0 availability will overlap for an extended period of time.

- Switch vendors can enable many of sRIO 2.0's benefits independent of available end points

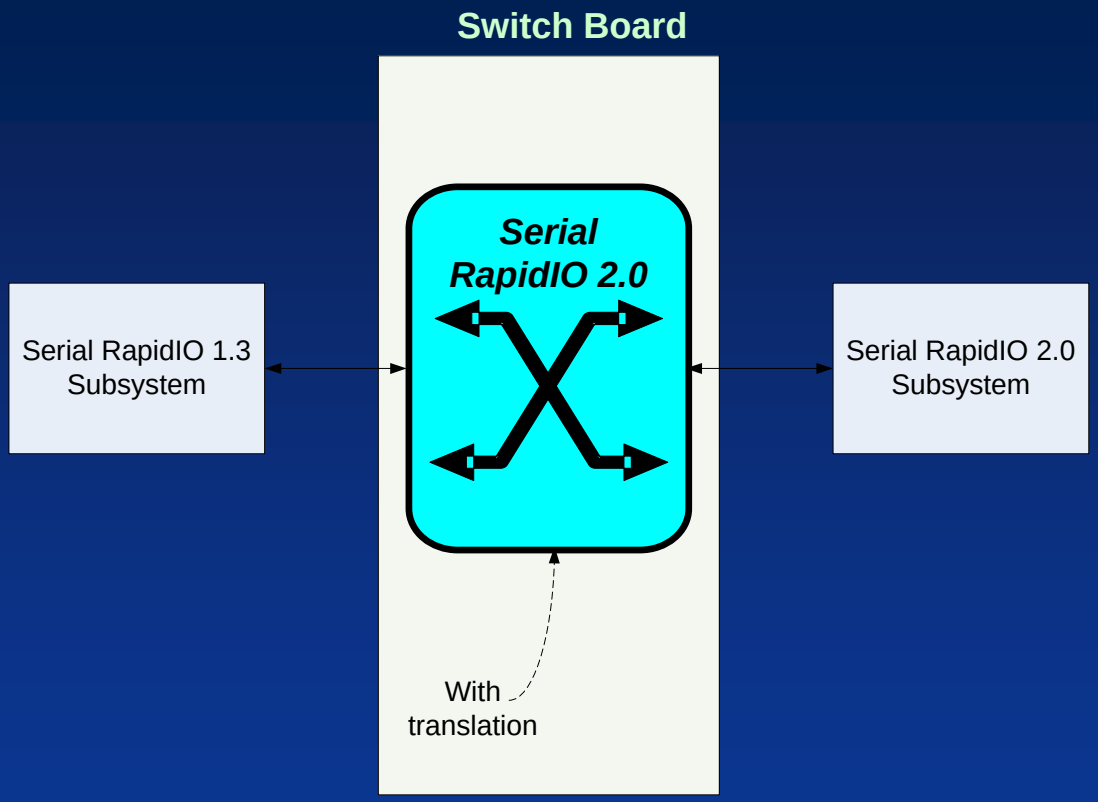
Mixed sRIO 1.3/2.0 System --- Example 1



- VC mapping in the input port
  - Using a unique destination identifier to assign VCs to the incoming packet

- Pseudo CT mode in the output side
  - A new packet replaces a packet that needs to be retransmitted.

Mixed sRIO 1.3/2.0 System --- Example 2

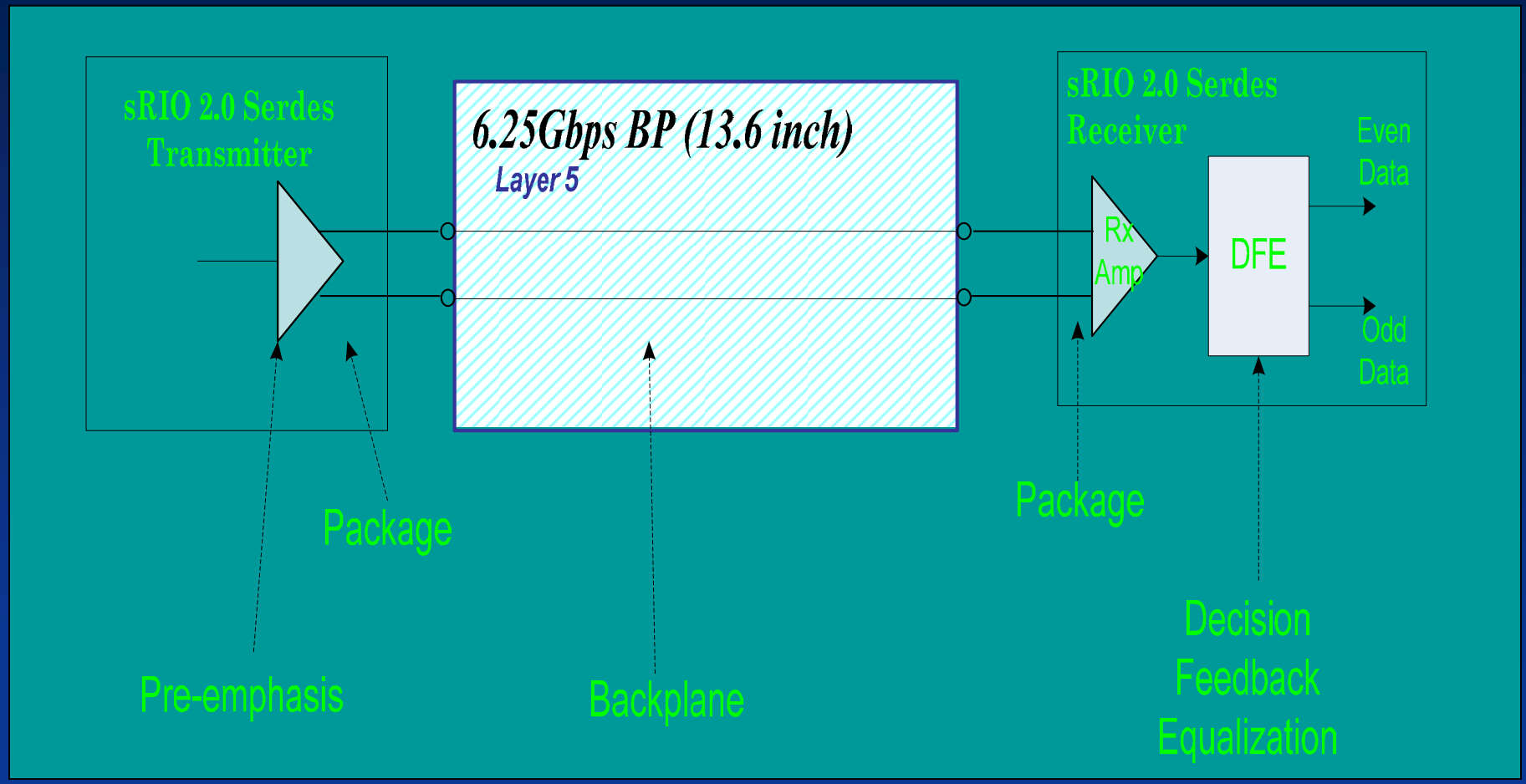


- Switch operates as a translator between sRIO 1.3 legacy traffic and sRIO 2.0 VC traffic.

Future Proofing your modular MicroTCA design for sRIO 2.0 tomorrow:

HSPICE Simulation with 13.6 inch BP at 6.25G

Hspice Simulation Architecture



22 Layer Backplane Stackup

Backplane

Overall Thickness: .138 +/- 10% Er (Dielectric Constant) = 3.5

		Dielectric		Copper		Target Impedance	Line / Space	Calc
	1		Signal	1.5	oz	50 to 75 ohms	.007	57.2
		.0053						
	2		Plane	.5	oz			
		.006				50 ohms +/- 10%	.00625	50.1
	3		Signal	.5	oz	100 Differential +/- 10%	.00625 / .020	99.91
		.0062						
	4		Plane	.5	oz			
		.006				50 ohms +/- 10%	.00625	50.1
	5		Signal	.5	oz	100 Differential +/- 10%	.00625 / .020	99.91
		.0062						
	6		Plane	.5	oz			
		.006				50 ohms +/- 10%	.00625	50.1
	7		Signal	.5	oz	100 Differential +/- 10%	.00625 / .020	99.91
		.0062						
	8		Plane	.5	oz			
		.006				50 ohms +/- 10%	.00625	50.1
	9		Signal	.5	oz	100 Differential +/- 10%	.00625 / .020	99.91
		.0062						
	10		Plane	.5	oz			
		.006				50 ohms +/- 10%	.00625	50.1
	11		Signal	.5	oz	100 Differential +/- 10%	.00625 / .020	99.91
		.0062						
	12		Plane	.5	oz			
		.006				50 ohms +/- 10%	.00625	50.1
	13		Signal	.5	oz	100 Differential +/- 10%	.00625 / .020	99.91
		.0062						
	14		Plane	.5	oz			
		.006				50 ohms +/- 10%	.00625	50.1
	15		Signal	.5	oz	100 Differential +/- 10%	.00625 / .020	99.91
		.0062						
	16		Plane	.5	oz			
		.006				50 ohms +/- 10%	.00625	50.1
	17		Signal	.5	oz	100 Differential +/- 10%	.00625 / .020	99.91
		.0062						
	18		Plane	.5	oz			
		.006				50 ohms +/- 10%	.00625	50.1
	19		Signal	.5	oz	100 Differential +/- 10%	.0625 / .020	99.91
		.0062						
	20		Ground	.5	oz			
New Layers		.002						
	21		Power	.5	oz			
		.003						
	22		Ground	1.5	oz			
		.1383	Final Thickness (After Plating)					

1) Approval of this stack-up supersedes fabrication drawing requireme
2) Some laminates require special order and additional lead time.

SI

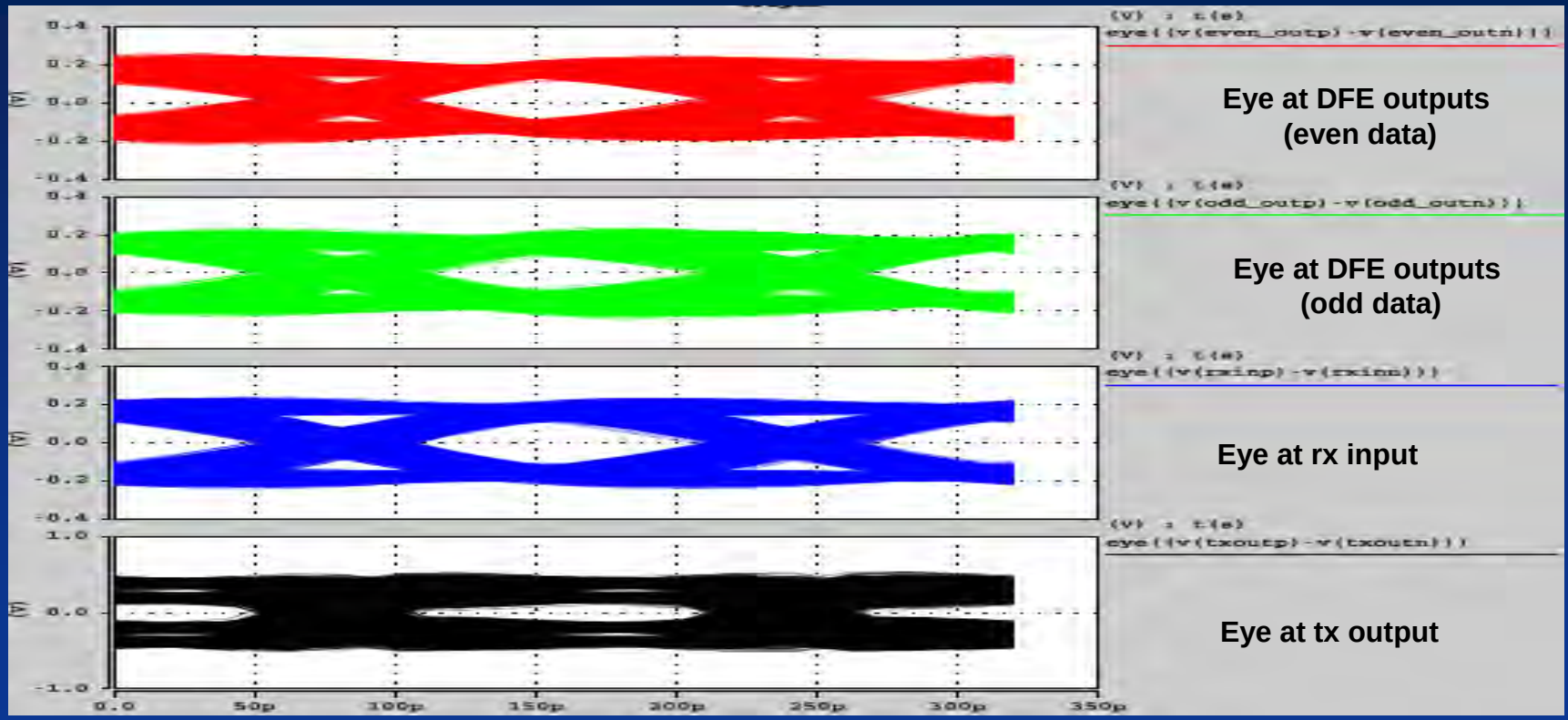
ε_R = 3.5

Tan δ = 0.008 @ 2.5 GHz

Electrical Properties		
Dielectric Constant (50% resin content)		
@ 1 GHz (RF Impedance)	3.7	3.4
@ 2.5 GHz (Split Post Cavity)	3.7	3.2
@ 10 GHz (Stripline)	3.6	3.2
@ 10 GHz (Split Post Cavity)	3.7	3.3
Dissipation Factor (50% resin content)		
@ 2.5 GHz (Split Post Cavity)	0.009	0.008
@ 10 GHz (Stripline)	0.009	0.008
@ 10 GHz (Split Post Cavity)	0.008	0.007

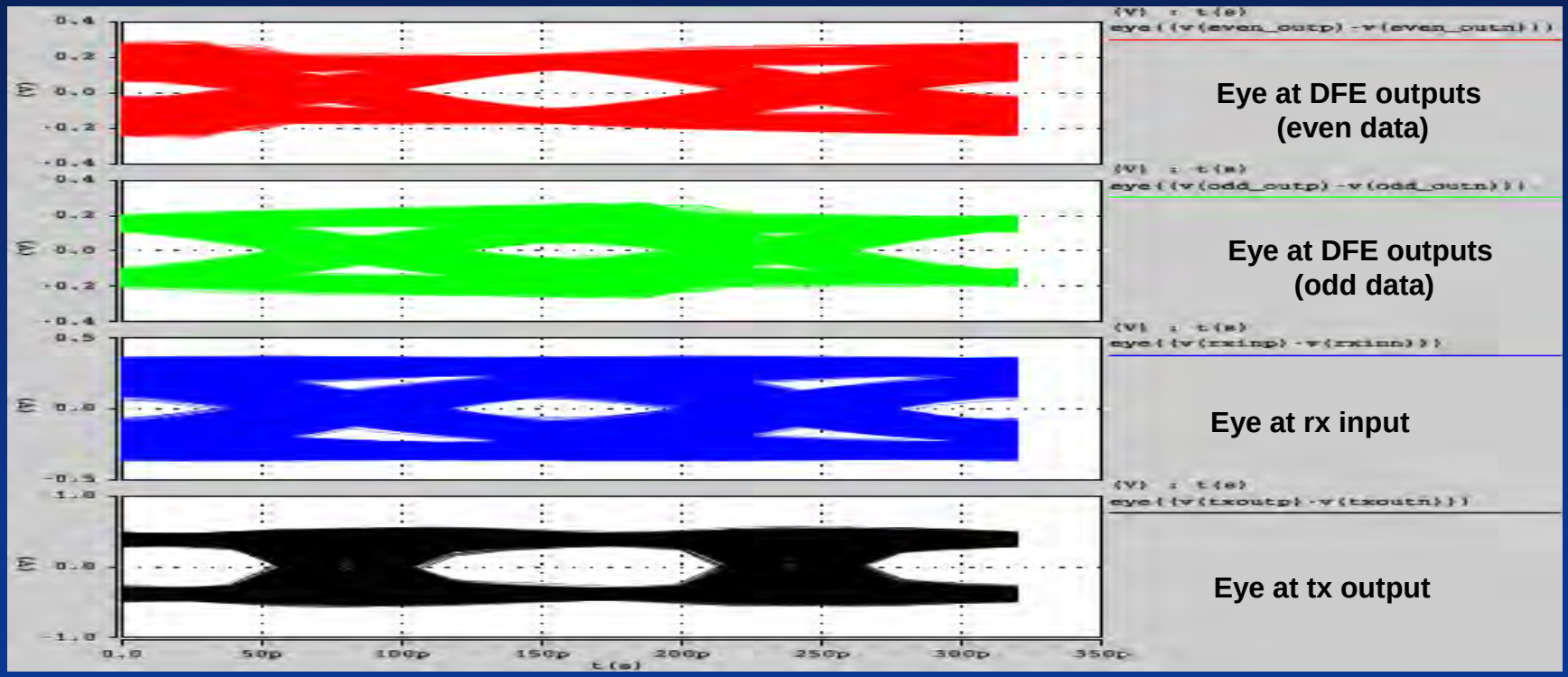
Layer 5 Escape: 6.25/20/6.25 Pair

6.25G eye Pre-emphasis Only, No DFE, No Package model



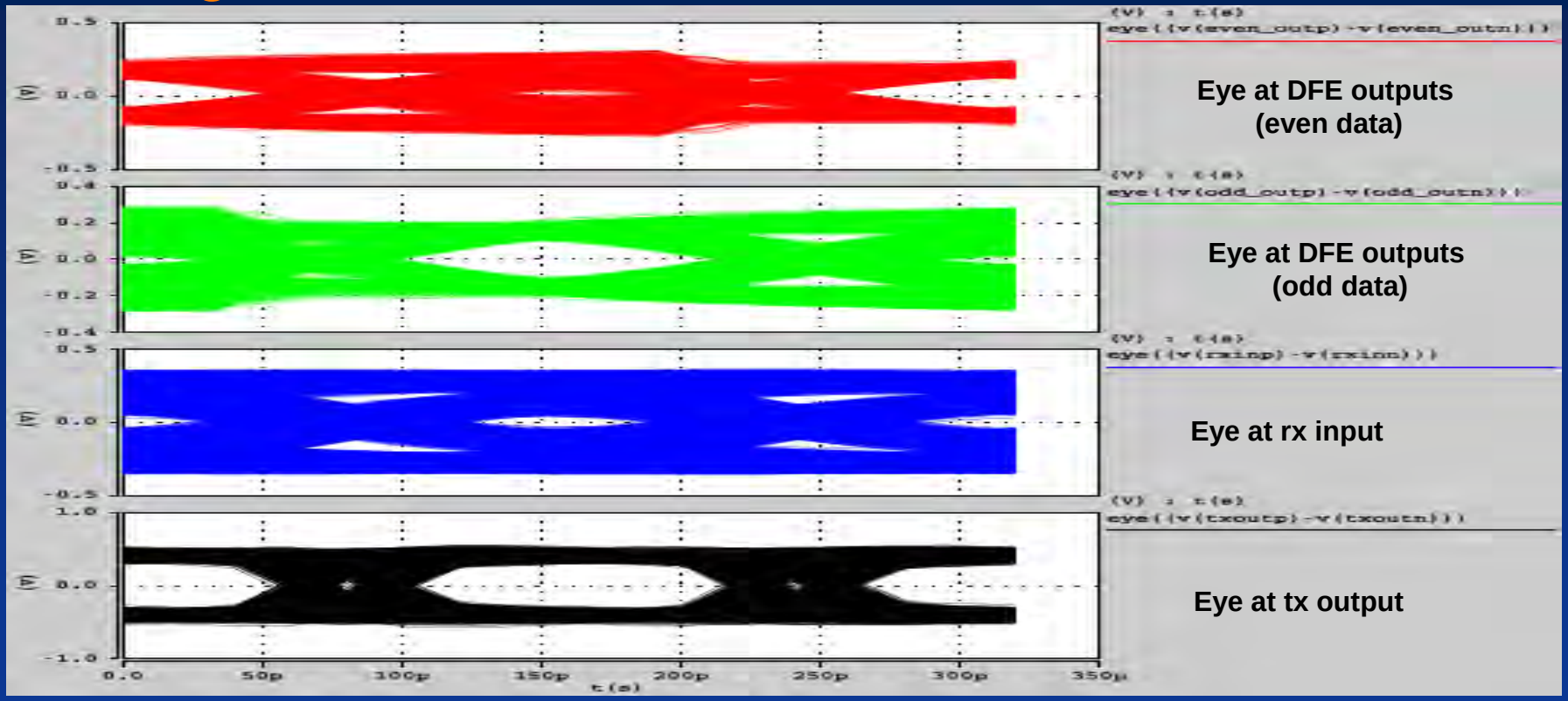
- **Tx pre-emphasis is able to open the eye at the input of Rx**

6.25G eye No Pre-emphasis, DFE On, No Package model



- **The eye at the Rx input got much smaller.**
- **However the DFE is able to open it up.**

6.25G eye No Pre-emphasis, DFE On, Plus Package model



- **The eye at Rx input is further reduced**
- **The DFE is able to open the eye nicely.**

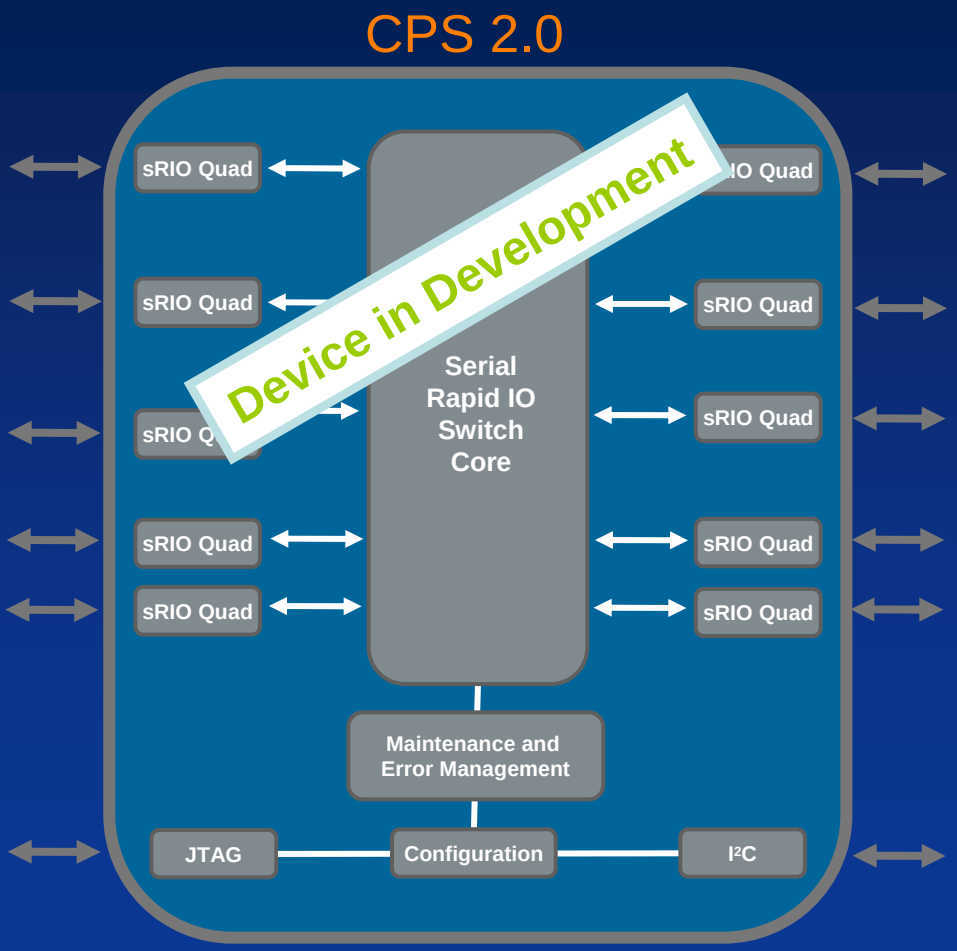
Hardware Proposal for MicroTCA system upgradeable to sRIO 2.0

- **Design will be MicroTCA based**
  - Cost-effective modular standard
  - Leverages existing infrastructure and COTS boards
  - sRIO 1.3 AMCs & MCHs are readily available now

- **MicroTCA backplane and cards designed for sRIO 2.0**
  - Can be designed today for a 12-slot backplane in FR4 @ 6.25G
  - Is a future-proof design for evolution from sRIO 1.3 to mixed sRIO to full sRIO 2.0
  - sRIO 2.0 components will be available ~2010

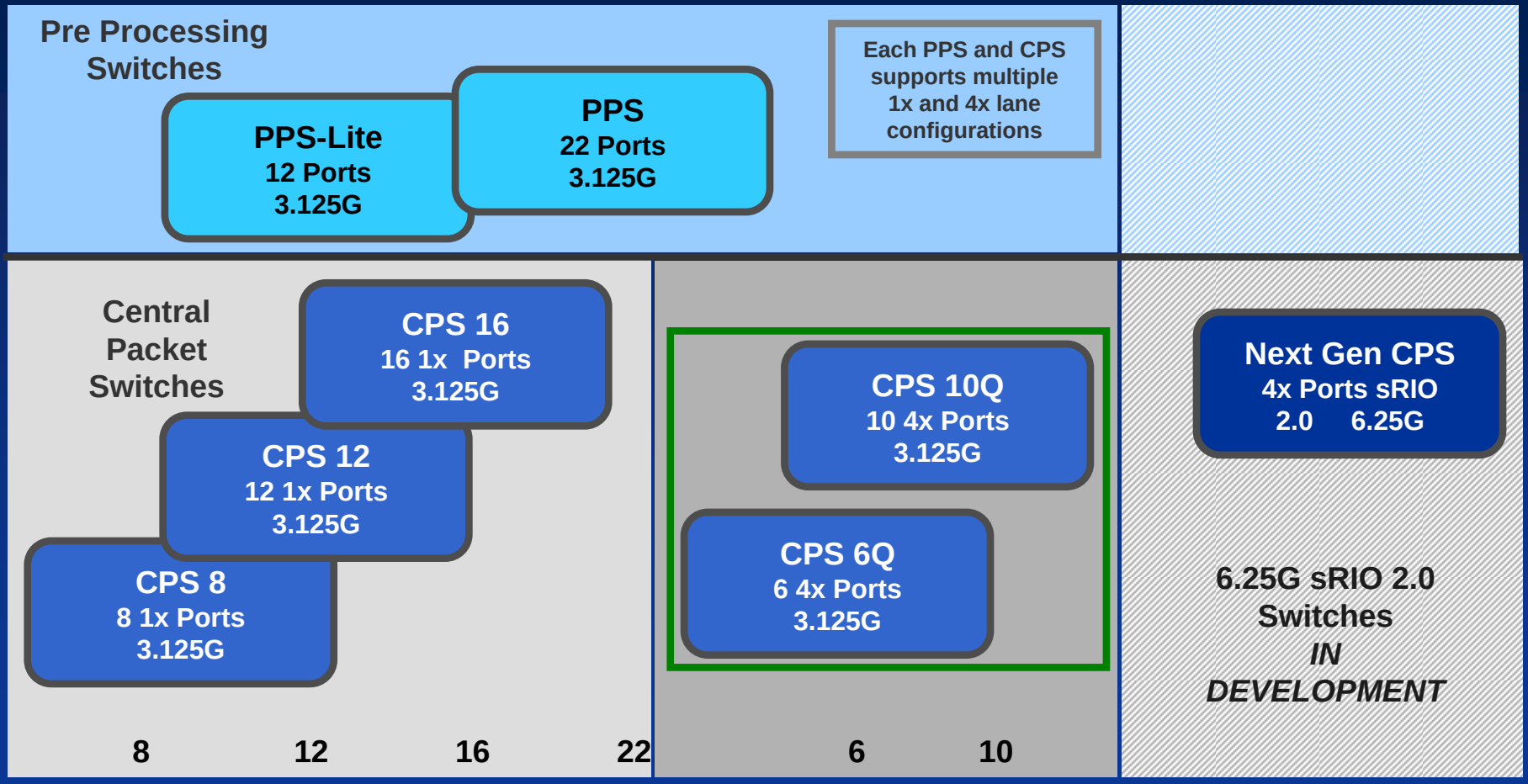
IDT - Leading The Transition to sRIO 2.0

3rd Generation CPS: Supporting 6.25G sRIO 2.0



- **Lanes**
  - All lanes will support 1.25, 2.5, 3.125, 5, and 6.25 Gbps
  - Backwards compatible with sRIO 1.3
- **Switch core performance**
  - Highest throughput
  - Lowest latency
- **Contact IDT for availability**

IDT - Expanding sRIO Switching Solutions



advanced TCA summit

THE END

Presenter

George Song is a senior application engineer in the Communications Division at IDT. He has more than ten years of experience in product development and customer support for a wide range of communications semiconductor solutions. George holds a Master's of Science in electrical engineering from the Harbin Engineering University of China. For more information, contact George Song at george.song@idt.com.

Additional Resources

RapidIO Trade Association: www.rapidio.org