

High-Speed Electronic Packaging Technology

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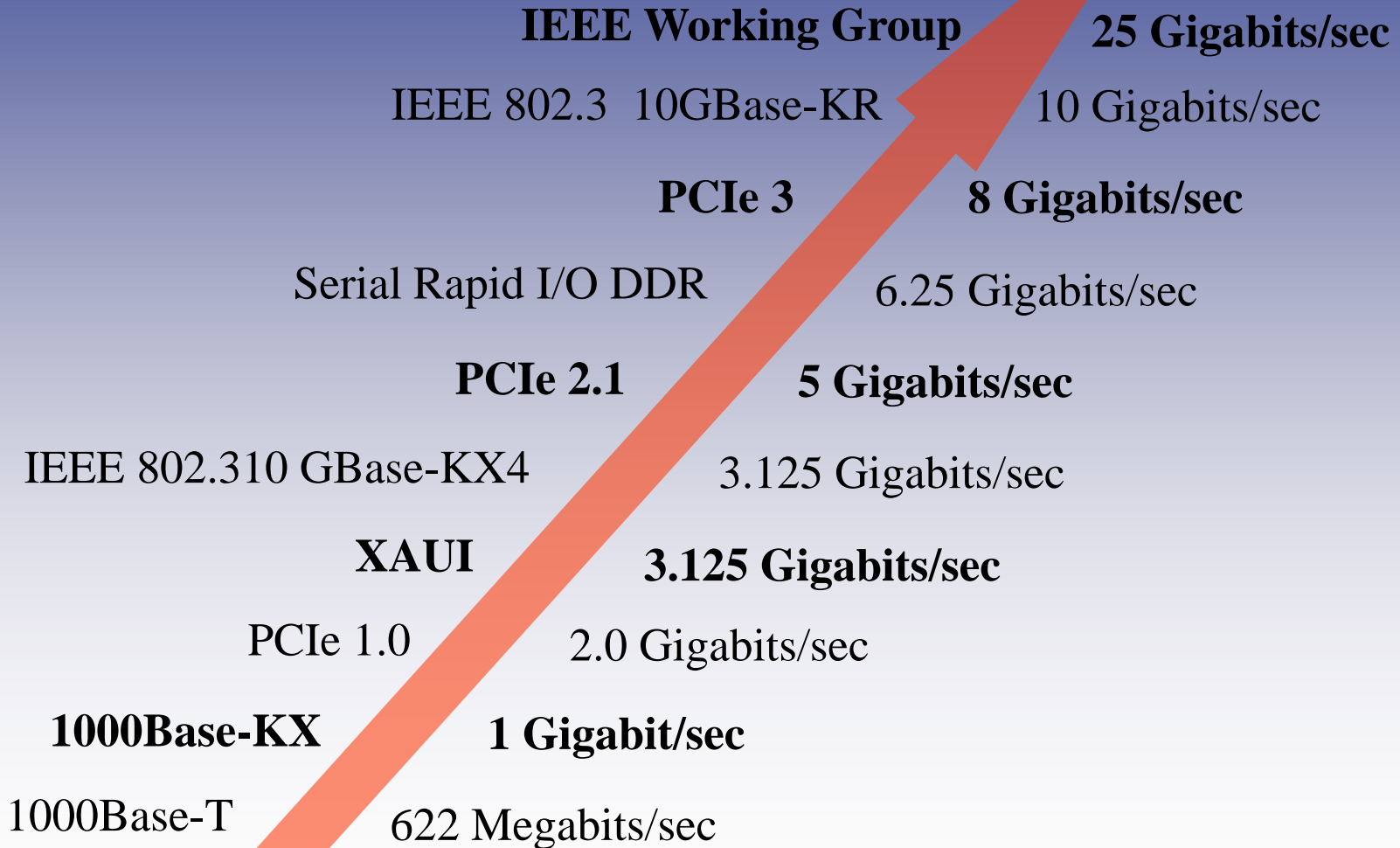
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ABSTRACT: New silicon implementing PCIe, SRIO, Infiniband and Ethernet are forcing standards bodies and trade associations to update channel requirements for backplane architectures supporting the new faster protocols. The traditional backplane has limitations that are well understood and each architecture is approaching the new backplane requirements in a similar way. The traditional approach is to reduce discontinuities by optimizing the trace geometries, in some cases reducing via diameters, back-drilling and using more expensive pcb dielectric layers. The current approach to the next generation backplane challenge is reviewed and the challenges of a traditional approach are explained.

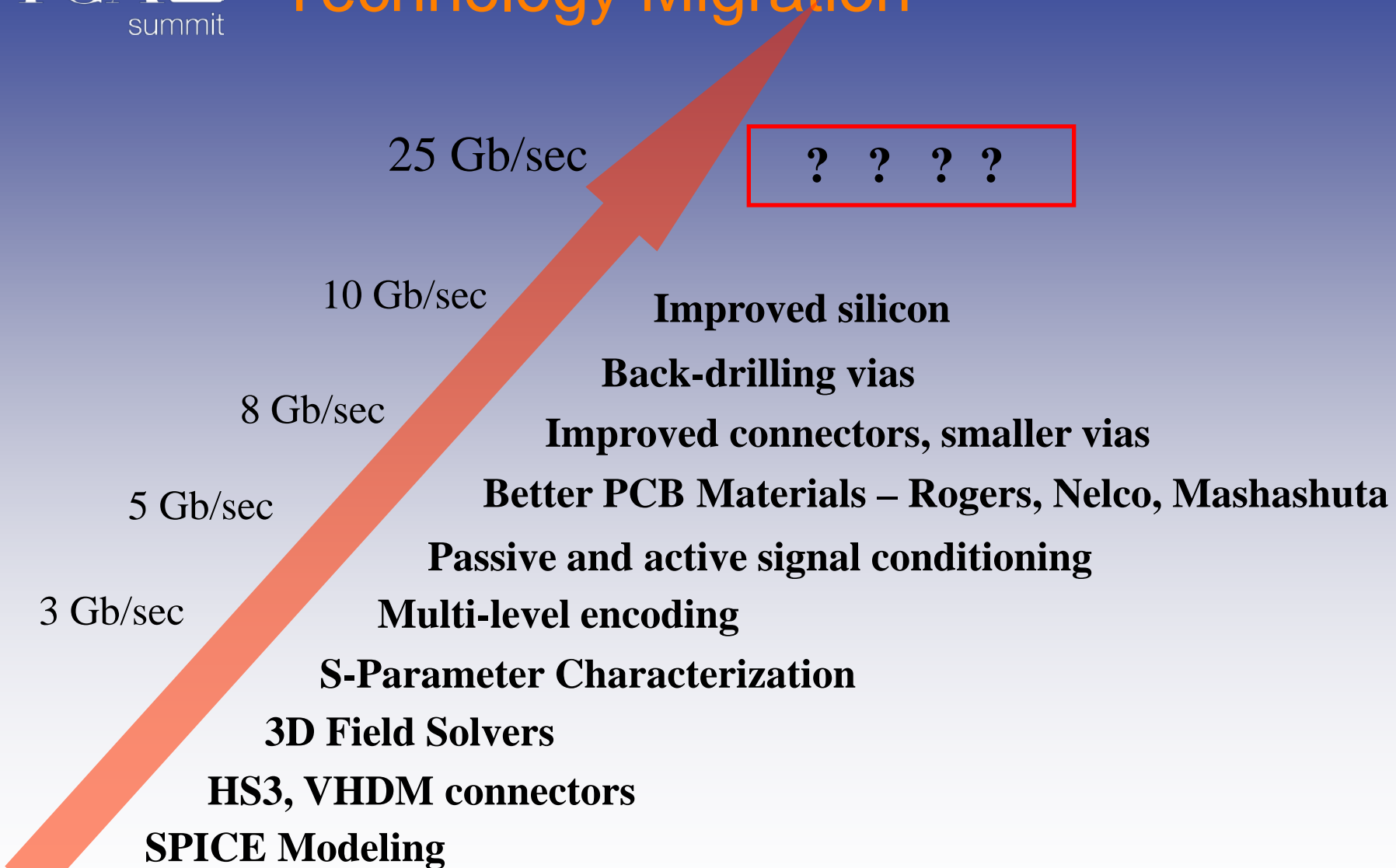
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Faster and Faster



Technology Migration



A New Approach – Z-Plane™

- Wider Traces
- Routing channels not limited by connector footprint
- Stripline construction
- Elimination of via stubs
- Backplane provides mechanical structure, power distribution and utility signals only (lower layer count)
- Requires ideal architectural topology
- Requires special rear connectors