

# MTCA.4 and PICMG 3.8

Two New Specifications  
*just released*

Bob Downing, chair

# Committee Cooperation!!

- I would like to thank the Companies and Laboratories world wide for the excellent cooperation in producing these specifications
- The process of working on MTCA.4 and PICMG 3.8 has been a privilege
- We had lots of ideas and help and may have set a record for finishing these documents
- Labs and companies prototyped early on and gave us confidence

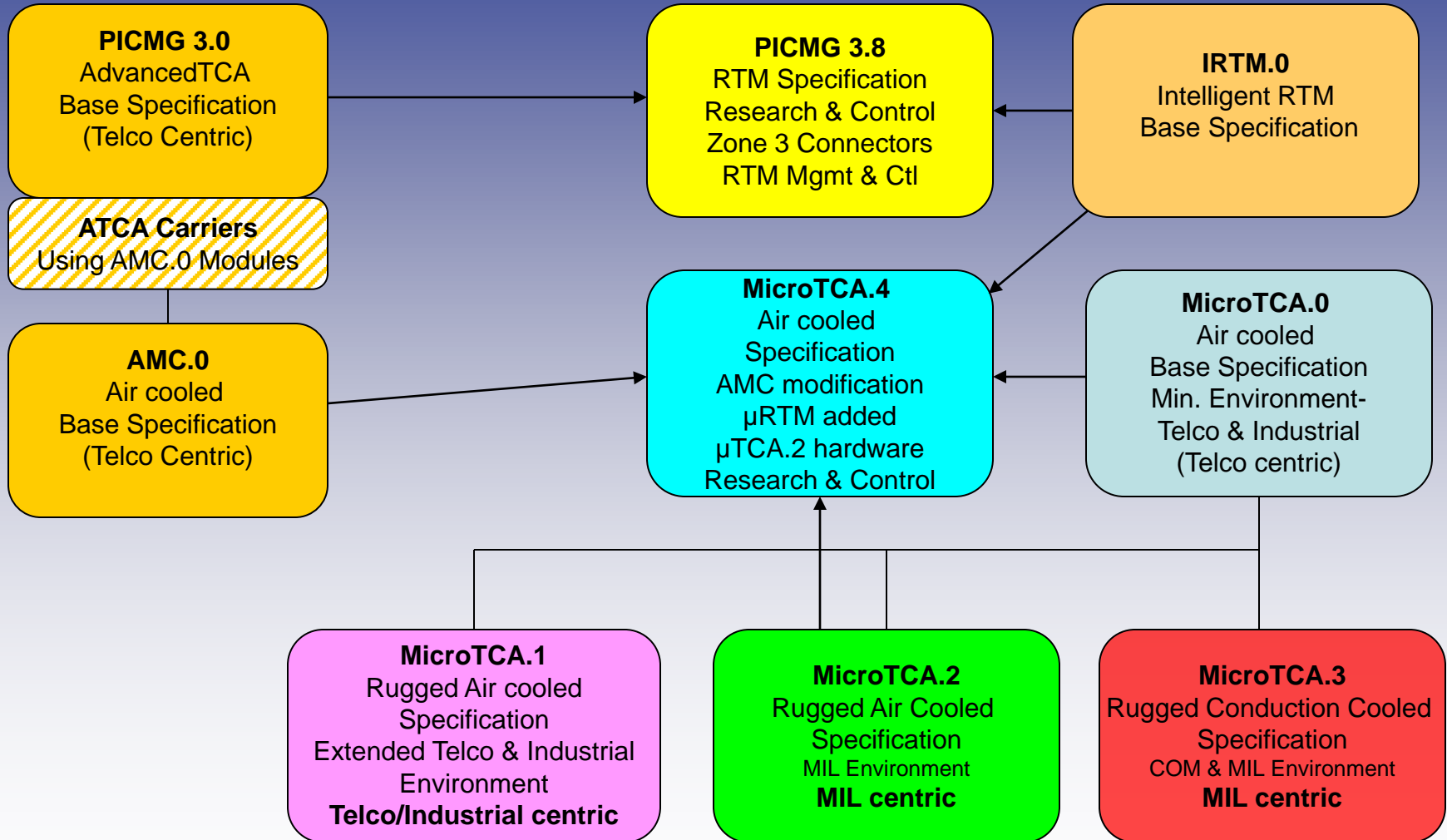
# Why is Physics into xTCA?

- The Physics research community uses standards widely in research.
- Standards make it easy to integrate systems that come from all over the world.
- xTCA specifications meet the requirements of:
  - Very high bandwidth
  - High availability
  - Integrated diagnostics

# Why did we want new features?

- High Energy Physics experiments have huge number of channels (sensors),  $10^6$  or more.
- High channel count makes rear I/O very attractive:
  - Ease of maintenance – front unobstructed
  - Less chance of cable and connector damage
  - Sensitivity of some cables to movement
- ATCA had rear I/O but only RTM mechanics
- $\mu$ TCA didn't have a  $\mu$ RTM

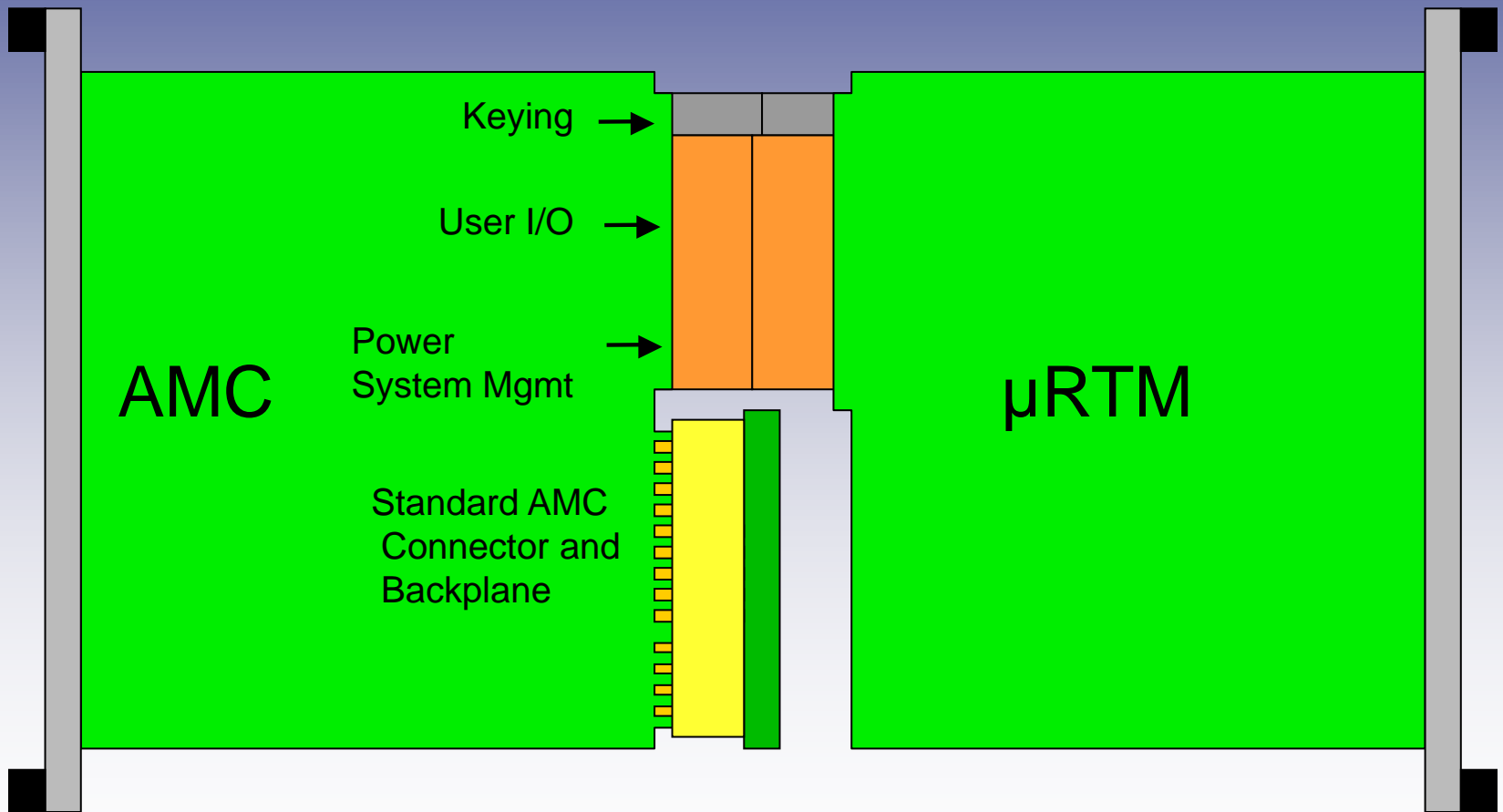
# The New Family Tree



# MicroTCA.4

- Specification defines:
  - Rear Transition Module
  - $\mu$ TCA shelf for AMCs and  $\mu$ RTMs
  - Defines the management system for the  $\mu$ RTM
  - Defines a new ADF variant (short pin) to accommodate live insertion
- All components were prototyped to validate the specification
- Several companies have shelves, AMCs and  $\mu$ RTMs available – check the exhibits

# AMC and $\mu$ RTM



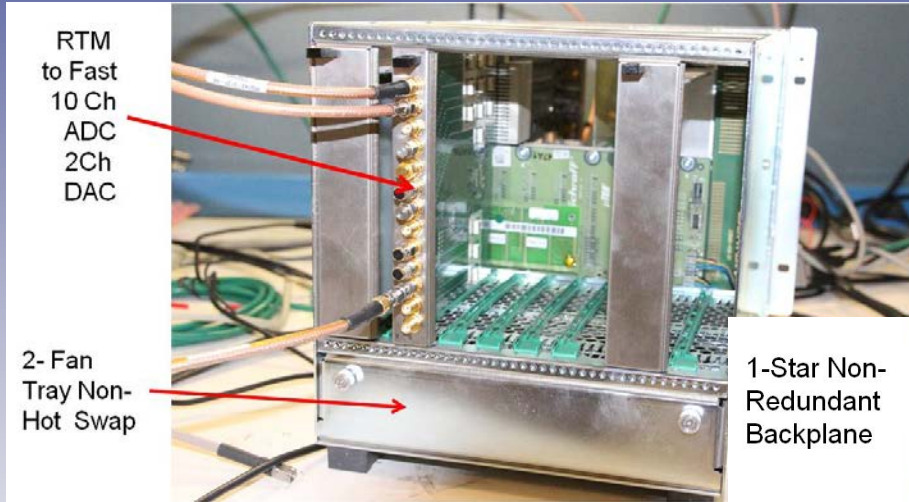
# μTCA Shelf Hardware

- Most μTCA shelf hardware is reused in the μRTM area to reduce cost
  - Card guide rails
  - Static discharge hardware
  - Panel hardware - Rugged version
- Fan cooling in rear specified to handle 30W per μRTM
- Separate front and rear fan control possible

# μRTM Hardware

- μRTM Module is nearly the same size as the front AMC
  - Mechanical parts from the current AMCs are reused
  - Parts rotated from top to bottom
- Panel for both AMC and μRTM is from the Rugged μTCA specification using retention screws
  - The mating forces for the Zone 3 connection exceeded the AMC latch
- The LED indicators are similar to those specified for the ATCA RTM

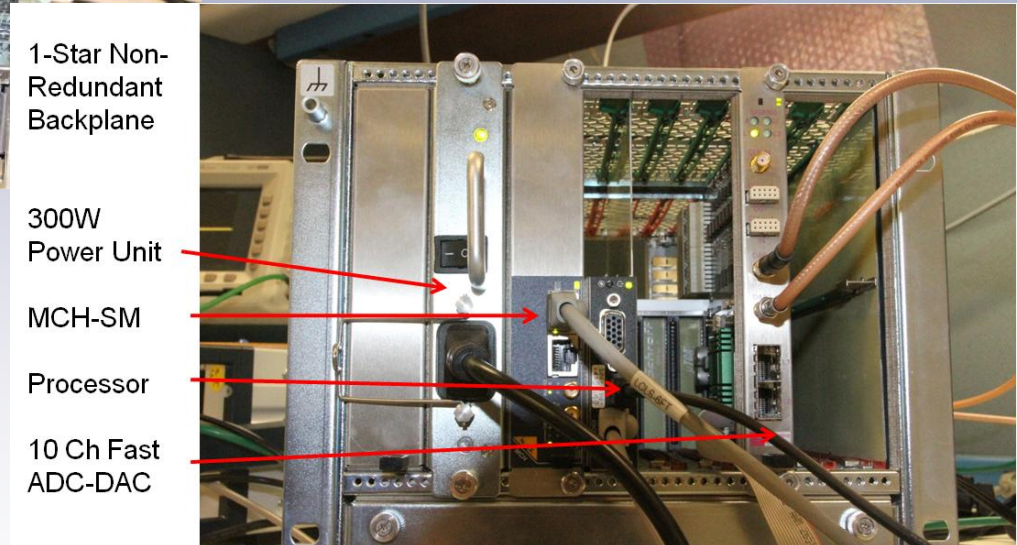
# 6 Slot MTCA.4 Shelf



↑ 6-Slot Rear View

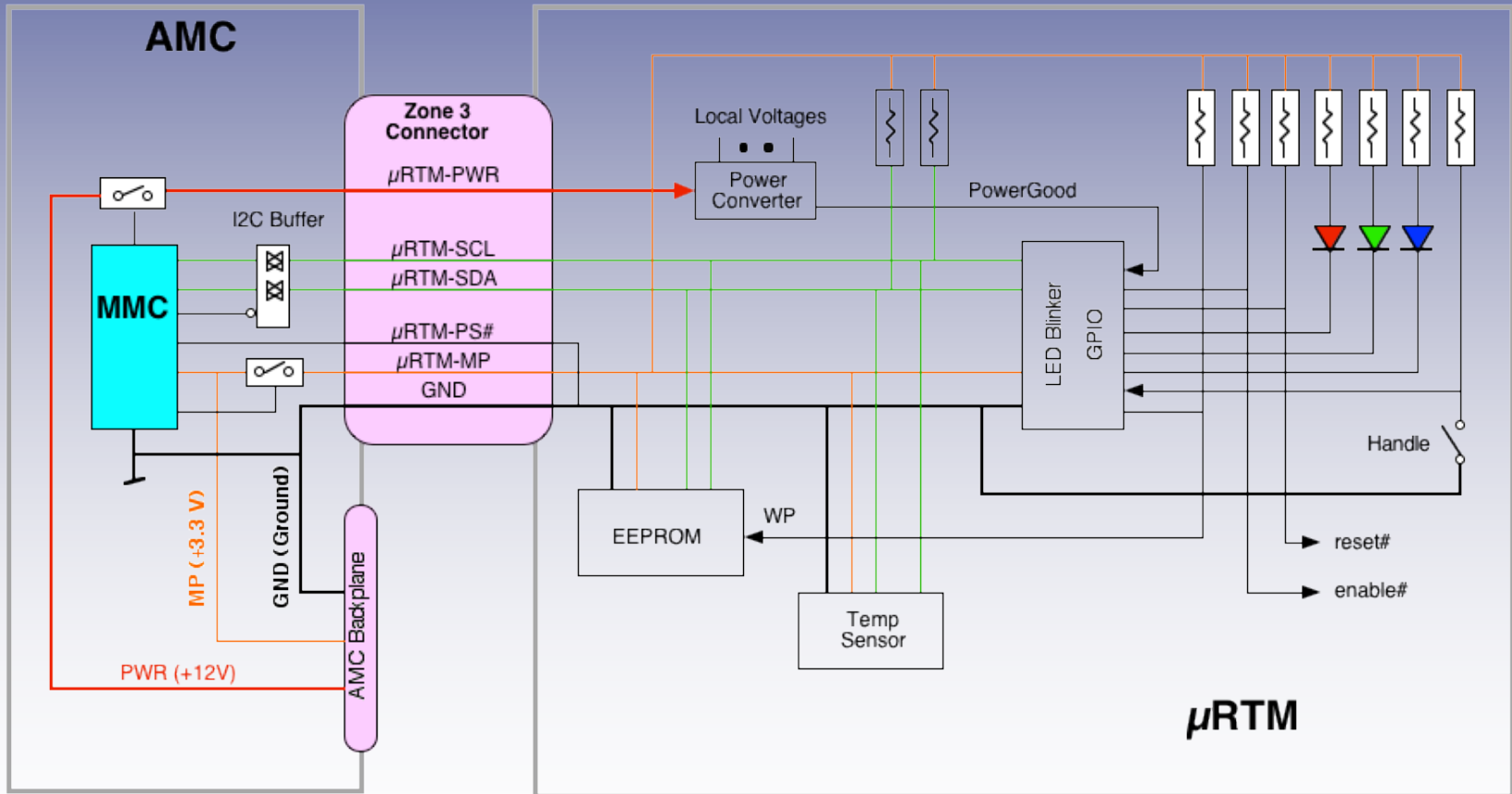
Courtesy Schroff, Struck

6 Slot Development Shelf  
 1-Star Non-Redundant  
 Front View



# MTCA.4 Management

- The AMC/ $\mu$ RTM pair are viewed as one unit from the system



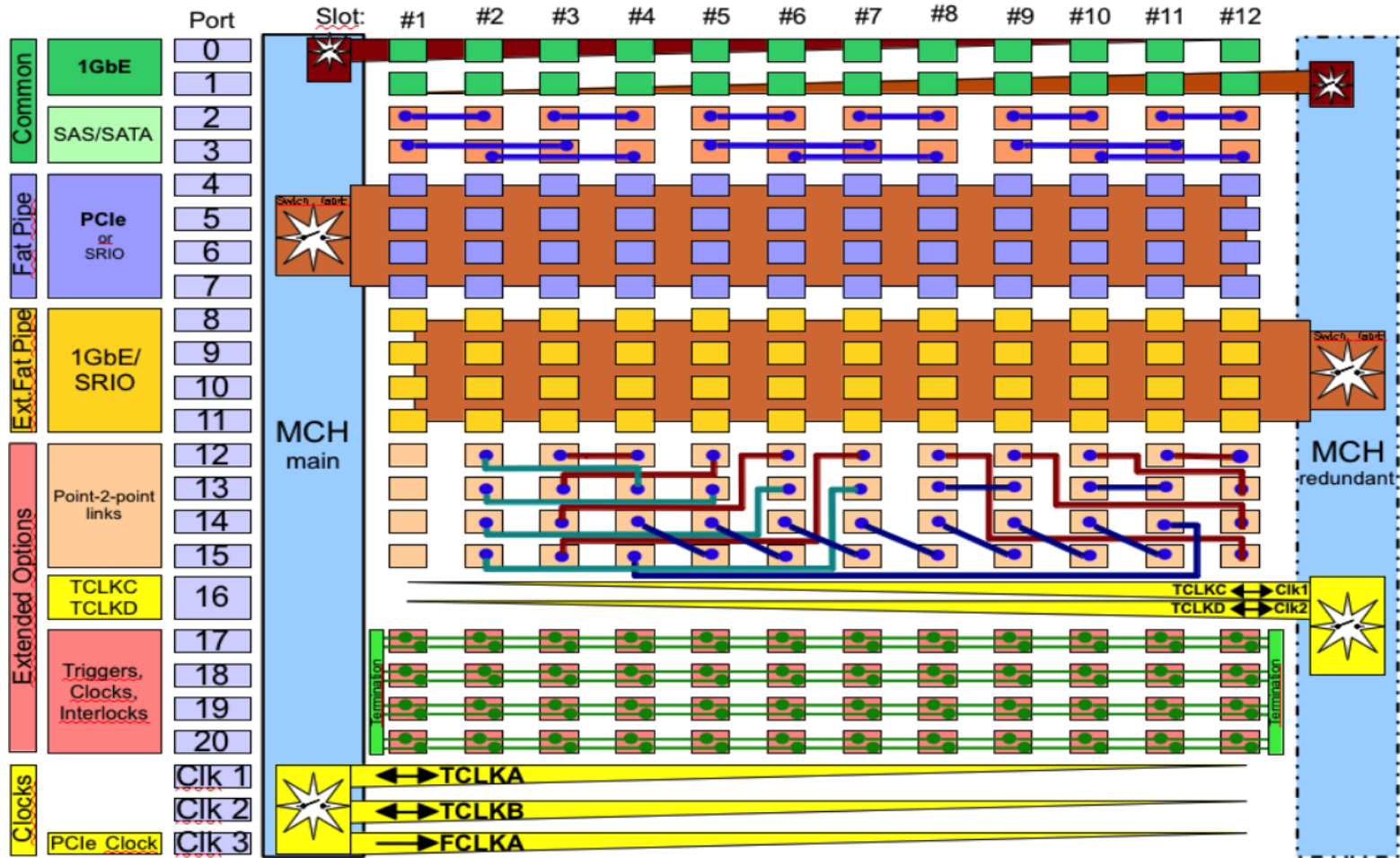
# μRTM Management Features

- Safety mechanical key implemented
- Short pin to indicate full insertion or removal
- 3v power is applied to μRTM if key matches
- μRTM has a serial PROM that communicates with the front AMC module's MMC
- Data read from the PROM is used by the system manager for enabling the μRTM 12v converter
- LED's, handle switch, *etc* are controlled and/or read thru the serial connection

# Physics Backplane Definition

- The Physics community needs certain module interconnect features in many research environments:
  - Interlocks
  - Analog summing of signals
  - Clock distribution
- A backplane is defined in MTCA.4 to accommodate these features
- Extended Options region used for Physics features
- Any AMC module that does not use this region will work in this backplane
- Physics backplane not required for  $\mu$ RTM

# MTCA.4 Backplane

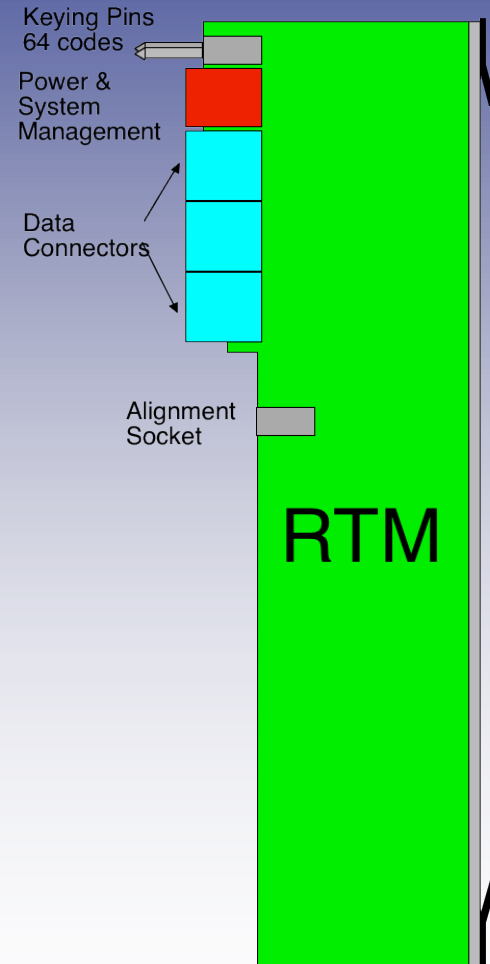


# PICMG 3.8

- PICMG 3.0 specified the mechanics for the RTM but no Zone 3 connectors
- As in MTCA.4 there is a need for specifying:
  - I/O connector in Zone 3
  - System connector
    - Power
    - Management
- IRTM specification in committee at the same time and helped with the Management definition in this specification

# RTM Mechanics Outline

- Alignment/Keying
- Power & System Management
- User I/O – ADF Connectors



# Management/Power Connector

- Connector defined in Zone 3 to perform similar function as Zone 1 connector
- Positronic Industries modified an existing connector that met the requirements
  - MP                      2 pins                      PWR                      4 pins
  - ENABLE#              1 pin                      PS#                      1 pin
  - SCL/SDA              2 pins                      JTAG                      4 pins
  - Reserved              2 pins

# Power

- MP specified to conform to AMC.0 R2.0 voltages and supply 500 mA minimum
- PWR specified to conform to AMC.0 R2.0 voltage tolerances and supply 5 A minimum
- The Reserved pins are placed so that the power can be increased in the future
- Other power requirements follow PICMG 3.0

# RTM Management

- This specification uses the management system defined in the PICMG IRTM.0
- The RTM appears to the system as if it were an AMC module.
- The optional Enable and PS# signals in the IRTM.0 specification are mandatory
- The PS# is a last mate pin for hot swap
- Identification codes are assigned to each RTM per the IRTM spec

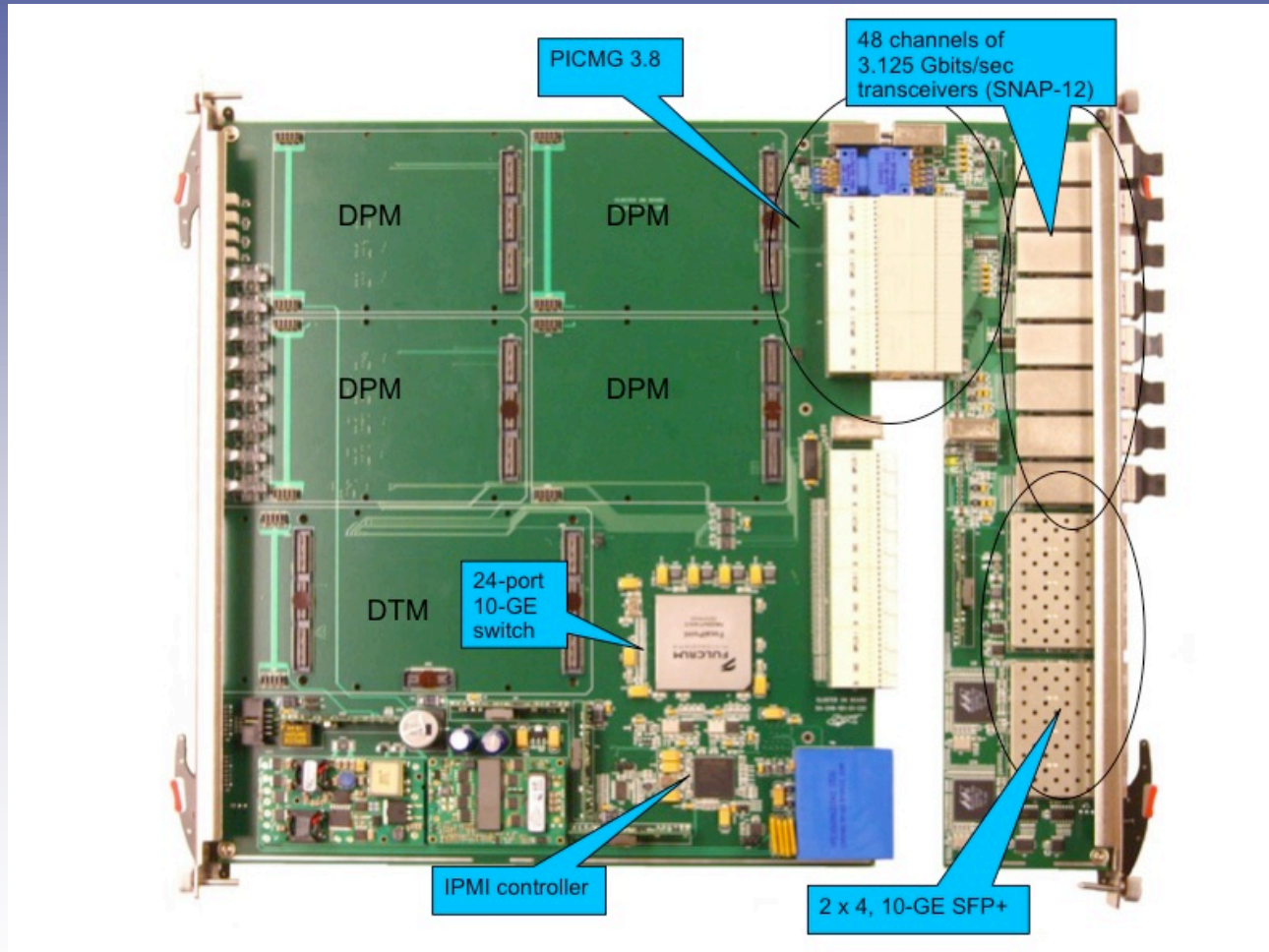
# Alignment & Keying

- ATCA specification defines alignment and two “keying” methods
- This specification defines mechanical keying codes that tell about the electrical interface
  - Mating is prevented if modules are not electrically compatible and damage could occur – mainly an analog signal issue
- After modules are mated the system management system checks the e-key to determine if modules are compatible and can be fully powered on

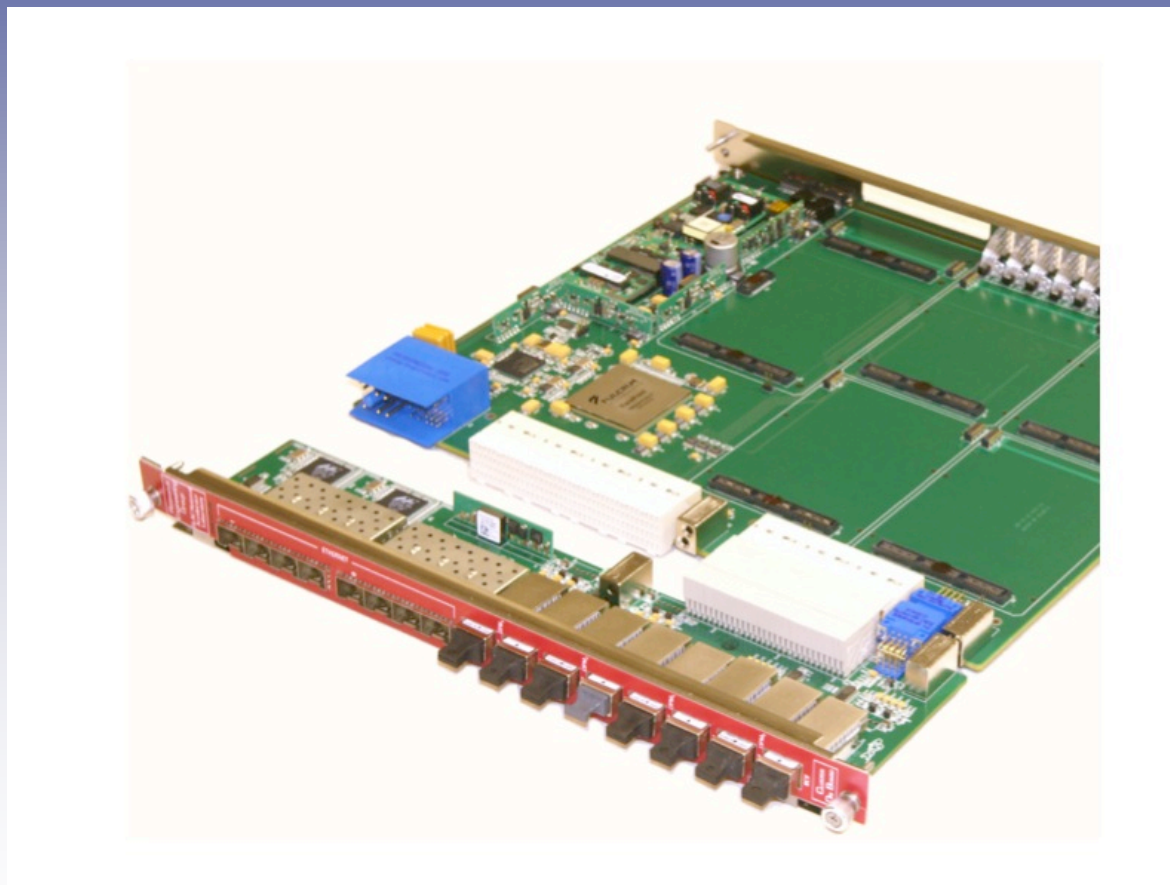
## User I/O

- The Physics RTM uses the same connectors as in Zone 2 of the ATCA specification
- There are up to 120 differential pairs or 240 single ended signals that can be connected between the ATCA module and its RTM
- Each pair has an associated ground pin
- A male right angle ADF has been specified, not in PICMG 3.8 and codes added to table

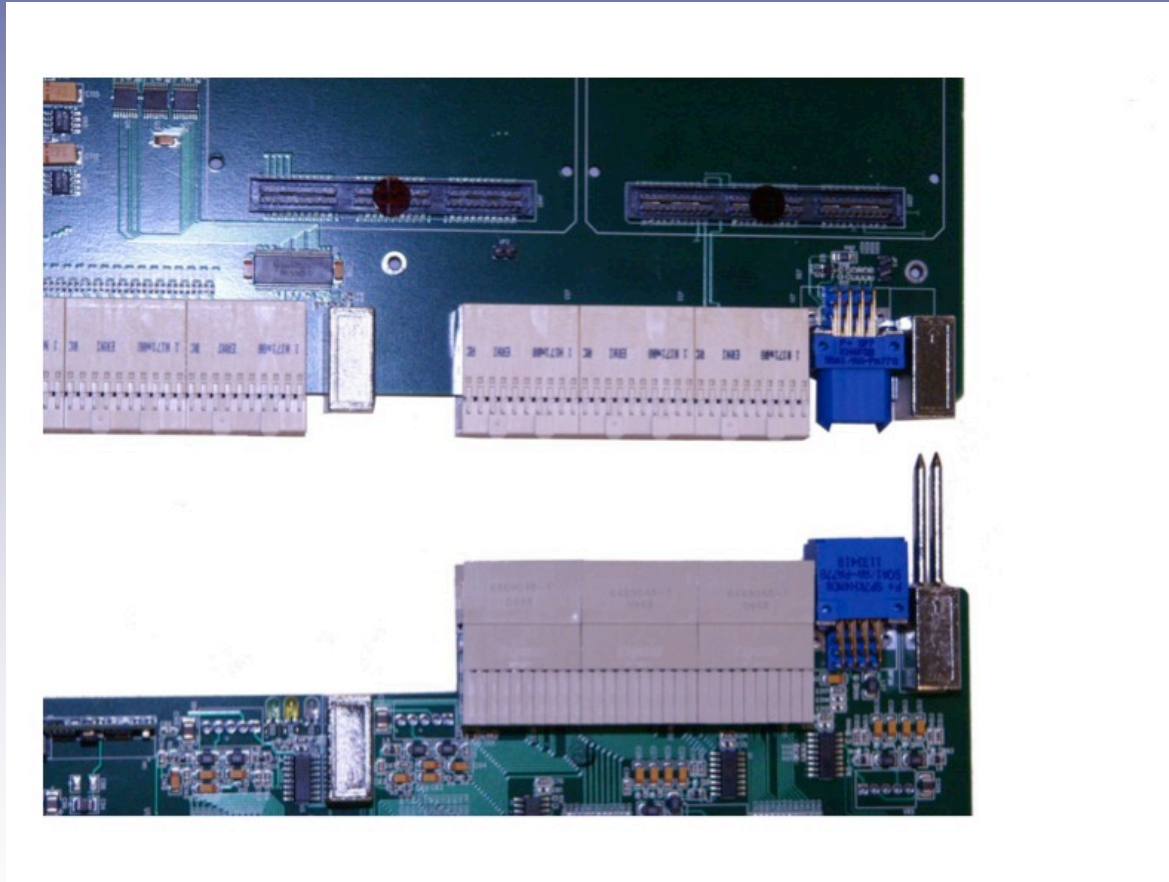
# SLAC COB (Cluster on Board)



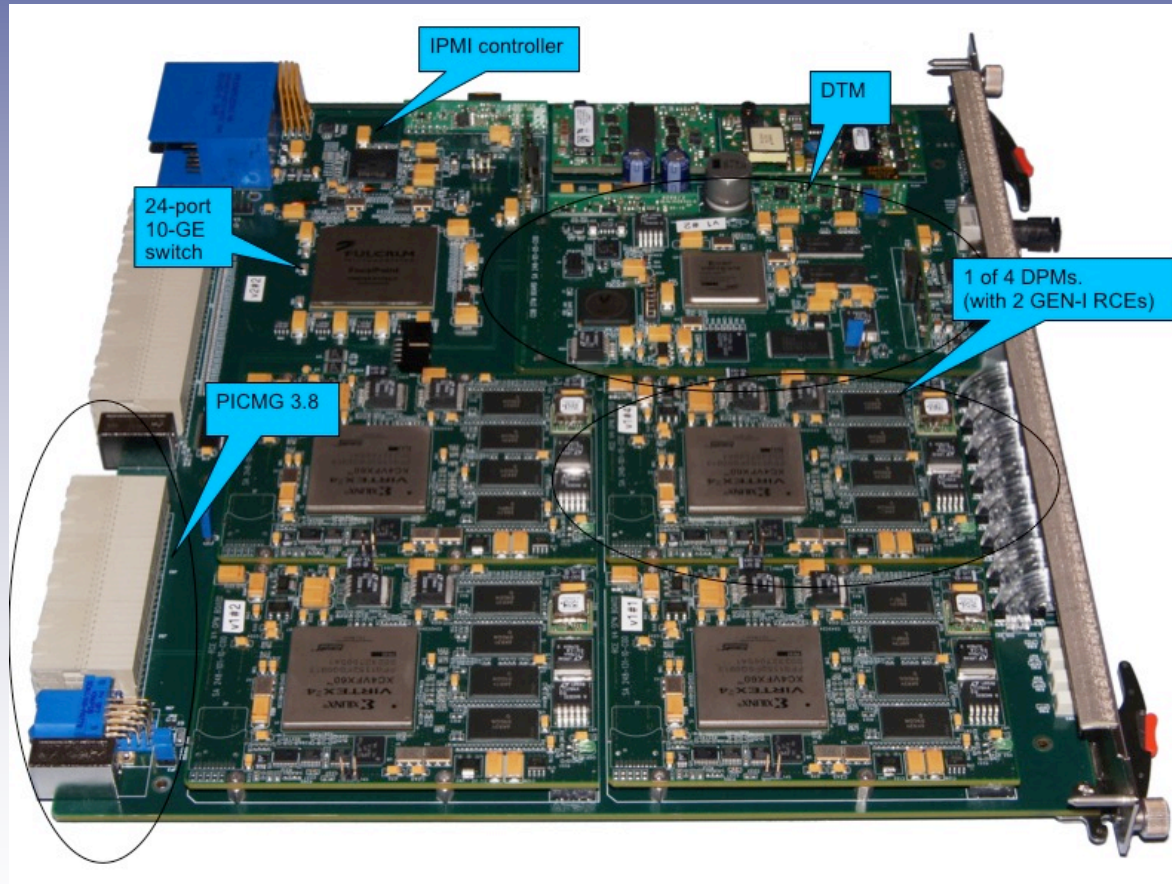
# SLAC COB-RTM



# SLAC COB- Zone 3



# SLAC COB – Populated



# COB Description

- The Front-Board is called COB (Cluster-On-Board). It is a full-mesh enabled, fully PICMG 3.0 compliant, node board. It contains a cluster of nine (9) RCEs. Each RCE is a generic computational unit, allowing users to "program" the RCE using arbitrary combinations of CPU, DSP, or combinatorial logic processing models. Each RCE contains:
  - A processor ( dual-core ARM Cortex A-9 operating at 1 GHZ with NEON APU and FP support),
  - 4 GBytes of DDR3 RAM (packaged in SO-DIMM)
  - up to 64 Gbytes of removable, flash based (microSD), persistent configuration memory.
  - A memory subsystem which sustains a bandwidth of up to 16 Gbytes/Sec (8 read and 8 write)
  - Generic, high speed serial I/O (up to 20 Serdes, each serdes capable of speeds up to 12.5 Gbits/sec
  - Generic, low-latency, high speed (the Protocol-Plug-In model") I/O model allowing synergy between processor fabric and external I/O
  - Housekeeping (I2C) interface allowing IPMI access to monitor and control each RCE (each mezzanine card appears as its own managed FRU)
  - Open Source, Real-time Kernel (RTEMS)- Software support for PPI services and bootstrapping (both development and resident)

# COB Description - cont

- The RCEs are all connected (clustered") together though a 10-GE switch.
  - Fully provisioned layer-3 switch, cut-through (lowest latency in the business, < 200 NS layer-2 switching, < 300 NS layer-3 switching)
  - 9 ports connect the RCEs on the board
  - 13 ports connect boards (through the fabric interface) as a full mesh thus allowing fully connected "clusters of clusters", or a shelf with sets of Ethernets.
  - 8 ports brought out to the RTM as SFP+
- The RTM is just one example of a "COB compliant" RTM. We believe there will be many depending on application. In this case its an RTM targeted for use on ATLAS. It contains:
  - PICMG 3.8 interface
  - Independent, hot swappable interface (appears as a managed FRU)
  - Contains as many as 8 SFP+
  - Contains as many as 48 channels of high-speed (3.2 Gbits/sec) fiber-optic transceivers (12/DTM).